WHAT IS CLAIMED IS:

1. An apparatus for manipulating ATM cells comprising:

a memory array in which an entire ATM cell can be read or written in one memory clock cycle; and

a mechanism for reading or writing the entire ATM cell from or into the memory array in one memory clock cycle.

2. An apparatus as described in Claim 1 wherein the memory array is comprised of N memory sub-arrays, where $N \geq 1$ and is an integer, each memory sub-array having rows and columns of memory cells, with there being enough memory cells to store all the bits of an ATM cell.

3. An apparatus as described in Claim 2 wherein at least one row or column has enough memory cells to store all the bits of an ATM cell.

4. An apparatus as described in Claim 3 wherein each row is RW bits wide and is greater than or equal to the number of bits in an ATM cell.

5. An apparatus as described in Claim 4 wherein each column is CW bits wide, where $CW \geq 1$.

6. An apparatus as described in Claim 5 wherein the reading or writing mechanism includes a row reading or writing mechanism for reading or writing the ATM cell into a row of the memory array.

7. An apparatus as described in Claim 6 wherein the reading or writing mechanism includes a mechanism for providing cells to the memory array, said providing mechanism in communication with the row reading or writing mechanism.

8. An apparatus as described in Claim 7 wherein the row reading or writing mechanism includes a row decoder mechanism for decoding and selecting a row of the memory array, said row decoder mechanism in communication with said memory array.

9. An apparatus as described in Claim 8 wherein the row reading or writing mechanism includes a mechanism for selecting a memory sub-array in communication with the memory array and the row decoder mechanism.

10. An apparatus as described in Claim 9 wherein the providing mechanism includes a W bus along which ATM cells travel to the memory array, said W bus connected to the selecting mechanism.

11. An apparatus as described in Claim 10 wherein the reading or writing mechanism includes a mechanism for delivering ATM cells from an ATM network to the W bus, said delivery mechanism connected with the W bus.

12. An apparatus as described in Claim 11 wherein the reading or writing mechanism includes a mechanism for transferring ATM cells from the W bus to an ATM network, said transferring mechanism connected with the W bus.

13. An apparatus as described in Claim 12 wherein the delivery mechanism includes a first mechanism for aligning the ATM cell so it is properly ordered to be written into the memory array

when it is delivered to the W bus, said first mechanism in contact with the W bus.

14. An apparatus as described in Claim 13 wherein the transferring mechanism includes a second mechanism for aligning the ATM cell so it is properly ordered after it is read from the memory array and transferred from the W bus to the ATM network, said second mechanism connected with the W bus.

15. An apparatus as described in Claim 14 wherein the mechanism for selecting a sub-array includes a memory sub-array row data selector for reading or writing a memory sub-array.

16. An apparatus as described in Claim 15 wherein the memory sub-array row data selector is comprised of N pass gate switch arrays, each pass gate switch array connected to a corresponding memory sub-array of the N memory sub-arrays, to the W bus and to the sub-array address decoder mechanism, said sub-array address decoder mechanism activating the pass gate switch array connected to the memory sub-array in which the ATM cell is to be written or read.

17. An apparatus as described in Claim 16 wherein each pass gate switch array comprised of RW pass gate switches, each pass gate switch connected to a corresponding column of the corresponding memory sub-array and to the sub-array address decoder mechanism.

18. An apparatus as described in Claim 17 wherein the first mechanism includes a plurality of cell vectorizing units which receive bits of an ATM cell from the ATM network and align them so they can be delivered in parallel to the W bus, said cell vectorizing units connected to the W bus, and a W-state machine

connected to the cell vectorizing units to control which cell vectorizing unit delivers its ATM cell to the W bus.

19. An apparatus as described in Claim 18 wherein the second mechanism includes a plurality of cell devectorizing units which receive bits of an ATM cell from the W bus in parallel and align them so they can be delivered to the ATM network, said cell devectorizing units connected to the W bus and the W-state machine, said state machine controlling which cell devectorizing unit receives an ATM cell from the W bus.

20. An apparatus as described in Claim 19 wherein each cell vectorizing unit is comprised of at least one layer of a plurality of registers in series which receive the bits of an ATM cell, and a cell vectorizing state machine connected to the registers and the W-state machine, said cell vectorizing state machine controlling which bits of the cell go to which register, determines when all the bits of an ATM cell are stored in the registers, and releases the bits of the ATM cell in the registers to the W bus when the W-state machine instructs it to do so.

21. An apparatus as described in Claim 20 wherein each cell devectorizing unit is comprised of at least one layer of a plurality of registers in series which receive the bits of an ATM cell from the W bus, and a cell devectorizing state machine connected to the registers and the state machine, said cell devectorizing state machine, determines when all the bits of an ATM cell are stored in the registers, and releases the bits of the cells in the registers to the ATM network.

22. An apparatus as described in Claim 21 wherein the W bus is comprised of RW bus lines, each bus line connected to a corresponding pass gate switch in each pass gate switch array.

23. An apparatus as described in Claim 22 wherein each register of the one layer of the cell vectorizing unit and the cell devectorizing unit is an 8-bit register having 8 register cells, each register cell holding a bit, each register cell connected to a corresponding bus line of the W bus.

24. An apparatus as described in Claim 23 wherein the W-state machine causes memory interleaving of the bits of the ATM cell when they are read from or written into the memory array, and wherein $H \leq RW$ and $H \leq CW$, where $H \geq 1$ and is an integer.

25. An apparatus as described in Claim 24 wherein 384 bits $\leq RW \leq$ 512 bits.

26. An apparatus as described in Claim 25 wherein the memory array is a 4 megabit DRAM having $N = 16$ memory sub-arrays and $CW = RW = 512$ bits.

27. An apparatus as described in Claim 28 wherein $1 \leq H \leq 256$.

28. An apparatus as described in Claim 27 wherein up to an additional 88 bits of data may be stored alongside an ATM cell.

29. A method for manipulating an ATM cell comprising the steps of:

providing an ATM cell to a memory array; and

writing the ATM cell into the memory array in one memory clock cycle.

30. A method as described in Claim 29 including after the writing step, there is the step of reading the ATM cell from the memory array in one clock cycle.

31. A method as described in Claim 30 wherein the writing step includes the step of writing the ATM cell into a row of the memory array.

32. A method as described in Claim 31 wherein the writing step includes the step of providing address information to identify the row in the memory array where the ATM cell is to be written.

33. A method as described in Claim 32 wherein the reading step includes the step of providing address information to identify the row in the memory array where the ATM cell is to be read.

34. A method as described in Claim 33 wherein the providing step includes the step of aligning the ATM cell with a W bus connected to the memory array.

35. A method as described in Claim 34 wherein after the aligning step, there is the step of transferring the ATM cell in one clock cycle to the W bus.

36. A method as described in Claim 35 wherein the providing address information step, there is the step of sending a control signal to desired pass gates connected to the memory array and the W bus bit of an ATM cell pass through the pass gate to a designated memory cell in the memory array.

37. A method as described in Claim 36 wherein the aligning step includes the step of storing bits of the ATM cell in registers in a CVU.

38. A method as described in Claim 37 including after the aligning step, there is the step of sending a sync cell ready signal to a W-state machine when the bits are properly aligned.

39. A method as described in Claim 38 wherein after the sending step, there is the step of sending a dequeue cell signal to the CVU state machine.

40. A method as described in Claim 39 wherein after the providing address information for reading includes the step of sending a sync ready for cell signal to the W-state machine from a CDU.

41. A method as described in Claim 40 including after the sending a sync ready for cell signal, there are the steps of sending a control signal to desired pass gates connected to the memory array and the W bus, and transferring the bits of the ATM onto the W bus from the memory array.

42. A method as described in Claim 41 including after the step of reading the bits, there are the steps of sending a cell_is_written signal to the CDU and storing the bits of the ATM cell in registers in the CDU in one clock cycle.

43. A method as described in Claim 42 after the step of storing the bits in the CDU, there is the step of reading each clock cycle from the registers and sending one byte then to an ATM network.

44. A method as described in Claim 43 including after the step of reading one byte, there is the step of transferring all remaining bytes of the ATM cell in a first layer of registers to a second layer of registers at a predetermined time.